Chapter 15
General Purpose Programmable Peripheral Devices

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Points to be Discussed

• 8255 Programmable Peripheral Interface
• 8254 (8253) Programmable Interval Timer
8255 Programmable Peripheral Interface Block Diagram
8255 Pin Diagram & Pin Description

Pin Configuration

<table>
<thead>
<tr>
<th>Pin</th>
<th>Number</th>
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<tbody>
<tr>
<td>PA0</td>
<td>4</td>
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<td>PA1</td>
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<td>PA2</td>
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<td>PA3</td>
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<td>PA5</td>
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<td>PA7</td>
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<tr>
<td>WR</td>
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<td>RESET</td>
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<td>D0</td>
<td>34</td>
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<tr>
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<td>PCU</td>
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<td>8255A</td>
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Pin Names

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
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<tbody>
<tr>
<td>D7–D0</td>
<td>Data Bus (Bidirectional)</td>
</tr>
<tr>
<td>RESET</td>
<td>Reset Input</td>
</tr>
<tr>
<td>CS</td>
<td>Chip Select</td>
</tr>
<tr>
<td>RD</td>
<td>Read Input</td>
</tr>
<tr>
<td>WR</td>
<td>Write Input</td>
</tr>
<tr>
<td>A0, A1</td>
<td>Port Address</td>
</tr>
<tr>
<td>PA7–PA0</td>
<td>Port A (Bit)</td>
</tr>
<tr>
<td>PB7–PB0</td>
<td>Port B (Bit)</td>
</tr>
<tr>
<td>PC7–PC0</td>
<td>Port C (Bit)</td>
</tr>
<tr>
<td>VCC</td>
<td>+5 Volts</td>
</tr>
<tr>
<td>GND</td>
<td>0 Volts</td>
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</table>
8255 Programmable Peripheral Interface

<table>
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<tr>
<th>CS</th>
<th>A₁</th>
<th>A₀</th>
<th>Selected</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Port A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Port B</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Port C</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Control Register</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>8255A is not selected.</td>
</tr>
</tbody>
</table>
8255 Chip Select & I/O Port Address
## 8255 Chip Select & I/O Port Address

<table>
<thead>
<tr>
<th><code>CS</code></th>
<th>Hex Address</th>
<th>Port</th>
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<tbody>
<tr>
<td>1 0 0 0 0 0</td>
<td>= 80H</td>
<td>A</td>
</tr>
<tr>
<td>0 1</td>
<td>= 81H</td>
<td>B</td>
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<tr>
<td>1 0</td>
<td>= 82H</td>
<td>C</td>
</tr>
<tr>
<td>1 1</td>
<td>= 83H</td>
<td>Control Register</td>
</tr>
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</table>
8255 Modes of Operation

Control Word

D7  D6  D5  D4  D3  D2  D1  D0

0/1

BSR Mode
(Bit Set/Reset)

For Port C
No effect on I/O Mode

I/O Mode

Mode 0
Simple I/O for ports A, B, and C

Mode 1
Handshake I/O for ports A and/or B
Port C bits are used for handshake

Mode 2
Bidirectional data bus for port A
Port B: either in Mode 0 or 1
Port C bits are used for handshake

(b)
8255 Control Word

Control Word

Group B
- Port C (Lower—PC₃–PC₀)
  - 1 = Input
  - 0 = Output
- Port B
  - 1 = Input
  - 0 = Output
- Mode Selection
  - 0 = Mode 0
  - 1 = Mode 1

Group A
- Port C (Upper—PC₇–PC₄)
  - 1 = Input
  - 0 = Output
- Port A
  - 1 = Input
  - 0 = Output
- Mode Selection
  - 00 = Mode 0
  - 01 = Mode 1
  - 1X = Mode 2

1 = I/O Mode
0 = BSR Mode
8255 Interfacing with 8085

HIGH LEVEL SENSOR

LOW LEVEL SENSOR

MOTOR

MOTOR DRIVER

8255

8085

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8255 Mode 0: Simple Input or Output

- In this mode, port A & B are used as two simple 8-bit I/O ports and port C as two 4-bit I/O ports.
- Each half of port C can be programmed as an input or output port.
- Features:
  - Outputs are latched.
  - Inputs are not latched.
  - Ports don’t have handshake or interrupt capability.
Mode 1: Input or Output with Handshake

• In this mode, handshake signals are exchanged between MPU and peripherals prior to data transfer.

• Features:
  – Ports A and B functions as 8-bit I/O ports. They can be configured either as input or output ports.
  – Each port uses three lines of port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions.
  – Input and output data are latched.
  – Interrupt logic is supported.

• In 8255A the lines of port C used as handshake signals vary according to the I/O function of a port.
Mode 1: Input Control Signals

- Port A uses: PC₃, PC₄ and PC₅.
- Port B uses: PC₂, PC₁ and PC₀.
- Functions of these signals:
  - **STB (Strobe Input):** This signal (active low) is generated by a peripheral device to indicate that it has transmitted a byte of data. The 8255A, in response to STB, generates IBF and INTR signal.
  - **IBF (Input Buffer Full):** This signal is an acknowledgment by the 8255A to indicate that the input latch has received the data byte. This is reset when MPU reads the data.
  - **INTR (Interrupt Request):** This is an output signal that may be used to interrupt the MPU.
  - **INTE (Interrupt Enable):** This is an internal flip-flop used to enable or disable the generation of the INTR signal. The INTEₐ is enabled or disabled through PC₄ and INTEₐ through PC₂.
  - **PC₆ and PC₇:** These two lines can be set up either as input or output.
Mode 1 (Input) Control and Status Words

(a) 8255
   - PA_7, PA_0, PC_4, PC_5, PC_3 → STB_A
   - PC_4, PC_5 → IBF_A
   - INTR_A

(b) Control Word—Mode 1 Input
   - D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0
   - I/O Mode
   - Port A Mode 1
   - Port A Input
   - PC_6, PC_7

(c) Status Word—Mode 1 Input
   - I/O, I/O, IBF_A, INTE_A, INTR_A, INTE_B, IBF_B, INTR_B

Port A with Handshake Signals
Port B with Handshake

Port B Input
I/O

I = Input
0 = Output
Mode 1 (Input) Timing Diagram

Mode 1 Port A

- PC4
- PC3
- PC6+7
- PORT A
- STB
- IBF
- INTR
- I/O

Mode 1 Port B

- PC2
- PC1
- PC0
- PORT B
- STB
- IBF
- INTR

Timing Diagram

- STB
- IBF
- INTR
- RD
- Port

Data strobed into port
Data read by microprocessor

(Buffer full)
(Interrupt request)

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Rahul Patel
Mode 1: Output Control Signals

- Port A uses: PC\textsubscript{7}, PC\textsubscript{6} and PC\textsubscript{3}.
- Port B uses: PC\textsubscript{2}, PC\textsubscript{1} and PC\textsubscript{0}.
- Functions of these signals:
  - **OBF (Output Buffer Full):** This is an output signal that goes low when MPU writes the data into the output latch of 8255. This signal indicates to an output peripheral that new data are ready to be read. It goes high again when 8255 receives the ACK signal.
  - **ACK (Acknowledge):** This is an input signal from a peripheral that must output low when the peripheral receives the data from 8255 ports.
  - **INTR (Interrupt Request):** This is an output signal that may be used to interrupt the MPU to request the next data byte for output.
  - **INTE (Interrupt Enable):** This is an internal flip-flop used to enable or disable the generation of the INTR signal. The INTE\textsubscript{A} is enabled or disabled through PC\textsubscript{6} and INTE\textsubscript{B} through PC\textsubscript{2}.
  - **PC\textsubscript{4} and PC\textsubscript{5}:** These two lines can be set up either as input or output.
Mode 1 (Output) Control and Status Words

(a) Diagram showing control signals for Port A and Port B.

(b) I/O Mode control signals for Port A and Port B.

(c) Status word diagram for Port A and Port B.
Mode 1 (Output) Timing Diagram

Mode 1 Port A
- INTE A
- PC6
- PC7
- PC3
- PC4+5
- PORT A
- ACK
- OBF
- INTR
- I/O

Timing Diagram
- WR
- OBF
- INTR
- ACK
- Port
- (Buffer full)
- (Interrupt request)
- Data sent to port
- Data removed from port

Mode 1 Port B
- INTE B
- PC2
- PC1
- PC0
- PORT B
- ACK
- OBF
- INTR

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Mode 2: Bidirectional Data Transfer

- In this mode, port A can be configured as the bidirectional port and port B either in mode 0 or mode 1.
- Port A uses five signals from port C as handshake signals for data transfer. The remaining signals from port C can be used either as simple I/O or as handshake signals for port B.
Mode 2: Bidirectional Data Transfer

Mode 2 and Mode 0 (Input)

Control Word
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
1 1 X X 0 1 I/O

PC_2-0
1 = Input
0 = Output

RD
WR

PC_3

PA_7-PA_0

8

INTRA

PC_7

OFRA

ACKA

PC_8

STBA

PC_4

PC_5

IBFA

PC_2-0

3

I/O

8

PB_7-PB_0

Mode 2 and Mode 1 (Output)

Control Word
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
1 1 X X 1 0 X

PC_3

PA_7-PA_0

8

OFRA

ACKA

PC_7

STBA

PC_4

PC_5

IBFA

PC_7-PB_0

8

PB_7-PB_0

INTRB

RD
WR
Bit Set Reset Control Word

FIGURE 15.6
8255A Control Word Format in the BSR Mode

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

0 X X X Bit Select S/R

BSR Mode

Not Used,
Generally Set = 0

Set = 1
Reset = 0

000 = Bit 0
001 = Bit 1
010 = Bit 2
011 = Bit 3
100 = Bit 4
101 = Bit 5
110 = Bit 6
111 = Bit 7
8254(8253) Programmable Interval Timer

• 8254 is a programmable timer/counter.

• Applications:
  – Generation of accurate time delays, square wave generation, real time clock, event counter, etc.

• Features:
  – It includes three identical 16-bit down counters
  – Six different operation modes.
  – It supports the count in both Binary/BCD format.
  – 8254 support the Read-Back Command for reading the count from the counter.
### Difference between 8253 and 8254

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<thead>
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<th></th>
<th>8253</th>
<th>8254</th>
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<tbody>
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<td>It can operates with</td>
<td><strong>clock frequency in the range from 0 (DC) to 2MHz</strong></td>
<td><strong>clock frequency in the range from 0 (DC) to 8MHz</strong></td>
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<tr>
<td><strong>It doesn’t include</strong></td>
<td><strong>Read-Back Command</strong> to latch the count of the counter before</td>
<td><strong>include Read-Back Command</strong> to latch the count of the counter</td>
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<tr>
<td><strong>Read-Back Command</strong></td>
<td><strong>reading.</strong></td>
<td><strong>before reading.</strong></td>
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# 8254 Control Word Format

<table>
<thead>
<tr>
<th>D7</th>
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<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>SC1</th>
<th>SC0</th>
<th>RW1</th>
<th>RW0</th>
<th>M2</th>
<th>M1</th>
<th>M0</th>
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<td>M2</td>
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<td>X</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>BCD</td>
</tr>
</tbody>
</table>

### SC—Select Counter:
- **SC1** | **SC0**
- 0 0: Select Counter 0
- 0 1: Select Counter 1
- 1 0: Select Counter 2
- 1 1: Read-Back Command (See Read Operations)

### RW—Read/Write:
- **RW1** | **RW0**
- 0 0: Counter Latch Command (see Read Operations)
- 0 1: Read/Write least significant byte only.
- 1 0: Read/Write most significant byte only.
- 1 1: Read/Write least significant byte first, then most significant byte.

### M—MODE:
- **M2** | **M1** | **M0**
- 0 0 0: Mode 0
- 0 0 1: Mode 1
- X 1 0: Mode 2
- X 1 1: Mode 3
- 1 0 0: Mode 4
- 1 0 1: Mode 5

### BCD:
- 0: Binary Counter 16-bits
- 1: Binary Coded Decimal (BCD) Counter (4 Decades)

**Note:** Don’t Care Bits (X) Should Be 0 to Ensure Compatibility with Future Intel Products.
8254 Modes

• Mode 0: **Interrupt on Terminal Count**
  - Once the count is loaded into the count register, the count is decremented every clock cycle and when the count reaches zero, the OUT goes high.
  - Gate = 0 halt the counting.
8254 Modes

• Mode 1: **Hardware Retriggerable One-Shot**
  
  - The OUT is initially high. When the Gate is triggered, the OUT goes low and at the end of the count the OUT goes high again.

![Diagram showing the waveforms for Mode 1 of 8254 modes](Image)
8254 Modes

- **Mode 2**: Rate Generator
  - When a count is loaded, the OUT stays high until the count reaches 1, and then the OUT goes low for one clock period.
  - The count is reloaded automatically and the pulse is regenerated continuously.

![Diagram of 8254 Mode 2](image)
8254 Modes

• Mode 3: **Square Wave Generator**
  - In this mode, when the count is loaded, the OUT high. The count is decremented by two at every clock cycle and when it reaches zero, the OUT goes low and the count is reloaded again. This is repeated continuously.
  - If the count \( N \) is odd, the pulse stays high for \( (N+1)/2 \) clock cycles and stays low for \( (N-1)/2 \) clock cycles.
8254 Modes

- **Mode 4**: **Software Triggered Strobe**
  - The OUT is initially high; it goes low for one clock period at the end of the count. The count must be reloaded for subsequent outputs.
8254 Modes

- **Mode 5:** Hardware Triggered Strobe
  - This mode is similar to Mode 4 except that it is triggered by the rising pulse at the gate.
  - At the end of the count, the OUT goes low for clock period.
Read Back Command

- It allows the user to read the count and status of the counter.
- This command is not available in the 8253.

(a) Read-Back Command Format

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>COUNT</td>
<td>STATUS</td>
<td>CNT 2</td>
<td>CNT 1</td>
<td>CNT 0</td>
<td>0</td>
</tr>
</tbody>
</table>

- D5: 0 = Latch Count of Selected Counter(s)
- D4: 0 = Latch Status of Selected Counter(s)
- D3: 1 = Select Counter 2
- D2: 1 = Select Counter 1
- D1: 1 = Select Counter 0
- D0: Reserved for Future Expansion; Must Be 0

A0, A1 = 11
CS = 0
RD = 1
WR = 0
**Status Byte read using Read Back Command**

<table>
<thead>
<tr>
<th>D_7</th>
<th>D_6</th>
<th>D_5</th>
<th>D_4</th>
<th>D_3</th>
<th>D_2</th>
<th>D_1</th>
<th>D_0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTPUT</td>
<td>NULL COUNT</td>
<td>RW1</td>
<td>RW0</td>
<td>M2</td>
<td>M1</td>
<td>M0</td>
<td>BCD</td>
</tr>
</tbody>
</table>

- **D_7**: 1 = Out Pin is 1  
  0 = Out Pin is 0
- **D_6**: 1 = Null Count  
  0 = Count Available for Reading
- **D_5-D_6**: Counter Programmed Mode
Thank you
Any Quarries?